

## CLAIMS

What is claimed is:

1. A Silicon on Insulator (SOI) device having an SOI region 310, a buried oxide region 312, and a P-Type inversion region 318, the P-type inversion region forming a first junction with the buried oxide layer and a second junction with the SOI layer, the buried oxide layer forming a third junction with the SOI layer, the P-type inversion region having a tongue 303 that extends into the third junction.
2. The device of claim 1 having a source 309 and drain 314 region and wherein the tongue 303 is closer to the source region 309 than to the drain region 314.
3. The device of claim 2 further comprising a handler wafer 304 biased at a voltage greater than said source voltage.
4. The device a claim 3 having a gate region 302, and wherein said gate 302 and said source 309 regions are biased at 50 or more volts less than said handler wafer 304, and wherein said drain voltage is biased at 50 or more volts greater than said handler wafer 304.
5. The device of claim 2 wherein said tongue 303 is comprised of Boron atoms.
6. The device of claim 5 wherein said boron atoms are implanted at a concentration of  $3 \times 10^{12}$  atoms/cm<sup>2</sup>.
7. A silicon on insulator (SOI) device having a an SOI layer 310, an adjacent buried oxide layer 312, and an inversion layer, the inversion layer 318 having an extension 330 that extends between the buried oxide layer 310 and the SOI layer 310.
8. The device of claim 7 wherein the extension is less than 1 micron in thickness.
9. The device of claim 7 wherein the extension comprises P-type doping.
10. The device of claim 9 wherein the extension comprises boron atoms.
11. The device of claim 9 further comprising source 309, drain 314, gate 302, and a wafer handler regions 304, and a voltage source connected to bias said wafer handler at a voltage less than that at which said drain is biased and greater than that at which said source is biased.
12. The device of claim 11 wherein said drain is biased at a voltage of approximately 200 volts higher than said source.
13. An SOI device comprising an N-Well region 316, a buried oxide region 312, and a P-inversion region 318, the P-inversion region 318 being extended into a junction

between said N-Well region 316 and said buried oxide region, said SOI device having a substrate region biased 304 at a voltage between a bias voltage applied to a source 309 of said device and a bias voltage applied to a drain 314 of said device.

14. The SOI device of claim 13 wherein a portion of the P-inversion region that extends into the junction is doped with charge in an amount such that it is depleted by the bias applied to the substrate layer.